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Attorney Docket Nº 01-956

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Andreev, Alexander E., et al.
Serial Nº	:	10/082,687
Filed	:	February 25, 2002
Group Art Unit	:	2167
Examiner	:	Robinson, Greta Lee
For	:	FFS SEARCH AND EDIT PIPELINE SEPARATION

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF AMENDED APPELLANT'S BRIEF

CERTIFICATE OF MAILING 37 C.F.R. § 1.8

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ReNea D. Berggren

ReNea D. Berggren DATED: July 11, 2005

Please find enclosed herewith one (1) copy of *Amended Appellants' Brief.*

This *Amended Appellant's Brief* is being filed in response to the *Notification of Non-Compliant Appeal Brief* dated June 27, 2005.

In the event that the Commissioner determines that any additional fees are required, or that any overpayment has been made, for this or any other Paper in this application, the Commissioner is hereby authorized to charge any such additional fees and to credit any overpayment to Deposit Account Nº 12-2252.

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PATENT

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In re application of	: Andreev, Alexander E.; Scepanovic, Ranko
Appl. No.	: 10/082,687
Filed	: February 25, 2002
Art Unit	: 2167
Examiner	: Robinson, Greta Lee
Title	: FFS SEARCH AND EDIT PIPELINE SEPARATION
Attorney Docket No.	: LSI 01-956

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AMENDED APPELLANTS' BRIEF

This is an appeal from the final Office Action dated February 14, 2005, rejecting claims 1-32.

(1) REAL PARTY IN INTEREST

The real party in interest is LSI Logic Corporation, the assignee of the entire interest.

(2) RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals, interferences or judicial proceedings.

(3) STATUS OF CLAIMS

The application was filed on February 25, 2002 with thirty-two (32) claims, of which Claims 1, 14 and 21 are independent.

All of the claims were rejected in the non-final Office Action dated July 16, 2004.

In Appellants' response dated September 13, 2004, Claims 1, 14 and 21 were amended, and arguments were made indicating the patentability of Claims 1-32 over the proffered references.

The Examiner rejected all the claims in the final Office Action dated February 14, 2005.

In Appellants' response dated March 16, 2005, arguments were made indicating the patentability of Claims 1-32 over the proffered references.

The Examiner, in the Advisory Action dated April 4, 2005, asserted that Appellants' arguments were not persuasive.

Appellants filed a Notice of Appeal dated April 21, 2005.

Appellants have received a Notification of Non-Compliant Appeal Brief dated June 27, 2005 from the Patent Office.

The status of the claims is as follows:

Claims rejected: Claims 1-32

Claims allowed: none

Claims withdrawn: none

Claims objected to: none

Claims canceled: none

Claims appealed: Claims 1-32

(4) STATUS OF AMENDMENTS AFTER FINAL

No amendment to the claims has been submitted since the final Office Action dated February 14, 2005.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1 provides:

A system (FIG. 1, reference character 100) suitable for providing a search comprising: a central controller (FIG. 1, reference character 102) suitable for implementing search and edit operations; and at least one search engine (FIG. 1, reference character 104, 106, 108 and/or 110) communicatively coupled to the central controller, wherein the central controller performs parallel execution of a search operation and an edit operation through utilization of a binary search tree and the at least one search engine (Specification, page 5, lines 4-27; Specification, page 6, line 13 to page 8, line 2; Specification, page 10, line 16 to page 11, line 2; FIG. 1, reference characters 100, 102, 104, 106, 108, 110, 116, 118, 120).

Independent Claim 14 provides:

A search engine (FIG. 2, reference character 200) suitable for providing a search, comprising: a memory (FIG. 2, reference character 202) suitable for storing electronic data; a priority controller (FIG. 2, reference character 208) communicatively coupled to the memory; an edit module (FIG. 2, reference character 206) communicatively coupled to the priority controller, the edit module configured to perform calculations for an edit operation; a search module (FIG. 2, reference character 204) communicatively coupled to the priority controller, the search module configured to perform calculations for a search operation; and an address cache (FIG. 2, reference character 210) communicatively coupled to the memory and the priority controller, the address cache suitable for storing electronic data; wherein the priority controller manages access to the memory by the edit module, search module and address cache, and the search engine provides the search using a binary search tree (Specification, page 5, lines 4-27; Specification, page 8, line 3 to page 10, line 15; FIG. 2, reference characters 200, 202, 204, 206, 208, 210).

Independent Claim 21 provides:

A system (FIG. 1, reference character 100) suitable for providing a search, comprising: a central controller (FIG. 1, reference character 102) suitable for implementing search and edit operations, the central controller suitable from inputting and outputting external communications; and a plurality of search engines (FIG. 1, reference characters 104, 106, 108, 110) arranged in zero through k levels, wherein k level search engine of the plurality of search engines is communicatively coupled to the central controller and a zero level search engine of the plurality of search engines is communicatively coupled to the central controller, wherein the central controller performs parallel execution of a search operation and an edit operation through utilization of a binary search tree and at least one of the plurality of search engines (Specification, page 5, lines 4-27; Specification, page 6, line 13 to page 8, line 2; Specification, page 10, line 16 to page 11, line 2; FIG. 1, reference characters 100, 102, 104, 106, 108, 110, 112, 114, 116, 118, 120).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Colbrook et al. ("Colbrook", Algorithms For Search Trees On Message Passing-Architectures) in view of Dixon et al. ("Dixon", U.S. Patent No. 4,464,718) and IBM Technical Bulletin entitled *Parallel Table Directed Translation* ("IBM").

(7) ARGUMENT

35 U.S.C. § 103(a) Rejections

I. Claims 1-2 and 21-22

The issue is whether the Examiner has properly rejected Claims 1-2 and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Colbrook et al. ("Colbrook", Algorithms For Search Trees On Message Passing-Architectures) in view of Dixon et al. ("Dixon", U.S. Patent No. 4,464,718) and IBM Technical Bulletin entitled *Parallel Table Directed Translation* ("IBM").

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (emphasis added) (MPEP § 2143). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. (emphasis added) *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Independent Claim 1 recites an element of "at least one search engine" (emphasis added). In rejecting Claim 1, the Examiner first admitted that Colbrook "do not show a search engine" (Final Office Action, page 3, line 7 form bottom). Then, the Examiner went on to allege that Dixon "teaches a search engine [note: search engine (controller 16) figure 1; abstract]" (Final Office Action, page 3, lines 5-6 from bottom). Appellants respectfully disagree.

Col. 4, lines 30-40 of Dixon recites:

> The host CPU 10 is connected via a bus 14 to an I/O controller 16. The functions of the I/O controller 16 include receiving data scan

> requests from the host CPU 10 (in the form of search request blocks as shown in FIG. 2), assembling the data necessary for performing the record scanning operation, and relaying the information necessary for performing the record scanning operation to the record scan circuit 20 and a device control unit 21 which is connected via bus 22 to a number of disk files 24A-24D (emphasis added).

In other words, "controller 16" in figure 1 of Dixon is an *I/O* controller and thus *cannot* be a search engine as recited in Claim 1. For the convenience of the Examiner, the search engine is illustrated, for example, in FIG. 2 and paragraph [0025] at page 8 of Specification of the present application.

The Examiner, in the Advisory Action dated April 4, 2005, asserted that "I/O controller which is a part of the search engine" (Advisory Action, page 2, last two lines). Appellants respectfully disagree. However, even if the Examiner's assertion were true, the I/O controller of Dixon still fails to teach, disclose, or suggest the search engine because the I/O controller of Dixon were just a *part* of the search engine, but *not* the search engine *itself.*

Since Colbrook, Dixon or IBM, individually or in combination, fails to teach, disclose, or suggest an element of "at least one search engine," as recited in Claim 1, it is respectfully submitted that a *prima facie* case of obviousness has not being established for Claim 1. Therefore, the rejection should be withdrawn, and Claim 1 is allowable.

Claim 2 depends from Claim 1 and is therefore allowable due to its dependence.

Independent Claim 21 recites an element of "a plurality of search engines" (emphasis added). Based on similar rationales as applied to Claim 1 (see above), Appellants respectfully submit that such element is not taught, disclosed, or suggested by Colbrook, Dixon, IBM, or any combination of them. Therefore, the rejection should be withdrawn, and Claim 21 is allowable.

Claim 22 depends from Claim 21 and is therefore allowable due to its dependence.

II. Claims 3-20 and 23-32

The issue is whether the Examiner has properly rejected Claims 3-20 and 23-32 under 35 U.S.C. § 103(a) as being unpatentable over Colbrook et al. ("Colbrook", Algorithms For Search Trees On Message Passing-Architectures) in view of Dixon et al. ("Dixon", U.S. Patent No. 4,464,718) and IBM Technical Bulletin entitled *Parallel Table Directed Translation* ("IBM").

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (emphasis added) (MPEP § 2143). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. (emphasis added) *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Claim 3 recites an element of "wherein the at least one search engine includes a priority controller, memory, edit module, search module and address cache" (emphasis added). In rejecting Claim 3, the Examiner has alleged that such element was taught by FIGS. 1-7 of Colbrook, and FIG. 1 and col. 4, lines 32-68 of Dixon. Appellants respectfully disagree. It is respectfully submitted that nowhere in the places pointed out by the Examiner was "a priority controller" taught, disclosed, or suggested. Appellants herein respectfully request the Examiner to pinpoint *exactly* where in Colbrook and Dixon was the element "a priority controller," as recited in Claim 3, taught, disclosed, or suggested. At least based on this reason, the rejection should be withdrawn, and Claim 3 is allowable.

Claims 4-13 depend from Claim 3 and are therefore allowable due to their dependence.

Claims 14 and 23 each recite an element of "a priority controller" (emphasis added). Based on the same rationale as applied to Claim 3 (see above), Claims 14 and 23 are allowable since Colbrook, Dixon or IBM, individually or in combination, fails to teach, disclose or suggest the element of "a priority controller," as recited in Claims 14 and 23.

Claims 15-20 depend from Claim 14 and are therefore allowable due to their dependence. Claims 24-32 depend from Claim 23 and are therefore allowable due to their dependence.

(9) CONCLUSION

For the foregoing reasons, it is respectfully submitted that in each of the rejections discussed herein under 35 U.S.C. § 103(a), the Examiner has failed to show that Colbrook, Dixon or IBM, individually or in combination, teaches or suggests each and every element of the claimed invention. Accordingly, reversal of all outstanding rejections is earnestly solicited.

Respectfully submitted,
LSI Logic Corporation,

Dated: July 11, 2005

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CLAIMS APPENDIX

1. A system suitable for providing a search, comprising:
a central controller suitable for implementing search and edit operations; and
at least one search engine communicatively coupled to the central controller, wherein the central controller performs parallel execution of a search operation and an edit operation through utilization of a binary search tree and the at least one search engine.

2. The system as described in claim 1, wherein the central controller and at least one engine are communicatively coupled via a search connection, an edit connection and a cache connection.

3. The system as described in claim 1, wherein the at least one search engine includes a priority controller, memory, edit module, search module and address cache.

4. The system as described in claim 3, wherein the priority controller manages access to the memory by the edit module, search module and cache module.

5. The system as described in claim 3, wherein the priority controller accesses data utilizing the address cache, the address cached configured to the address cached configured to receive data from the memory.

6. The system as described in claim 3, wherein the edit module connects with the memory through the priority controller, the edit module configured to perform calculations for editing operations.

7. The system as described in claim 3, wherein the search module is configured to perform calculation for a search operation.

8. The system as described in claim 7, wherein the search module is communicatively connected to a second search module of a second search engine positioned at a

neighboring level, the second search engine positioned at least one of at a previous or subsequent level to the search module.

9. The system as described in claim 7, wherein the search engine is a 0th level search engine, output of the search module is provided to the central controller and wherein the search engine is a top search engine, the input of the search module is obtained from the central controller.

10. The system as described in claim 3, wherein the edit module has inputs and outputs from a neighboring search engine level to the search engine.

11. The system as described in claim 3, wherein the priority controller gives priority to a search operation over an edit operation.

12. The system as described in claim 3, wherein the priority controller accesses the address cache to provide parallel access.

13. The system as described in claim 12, wherein the priority controller receives a request to read a memory address of the memory, content of the memory address is copied to a first cache address and a second cache address of the address cache.

14. A search engine suitable for providing a search, comprising:
a memory suitable for storing electronic data;
a priority controller communicatively coupled to the memory;
an edit module communicatively coupled to the priority controller, the edit module configured to perform calculations for an edit operation;
a search module communicatively coupled to the priority controller, the search module configured to perform calculations for a search operation; and
an address cache communicatively coupled to the memory and the priority controller, the address cache suitable for storing electronic data;
wherein the priority controller manages access to the memory by the edit module, search

module and address cache, and the search engine provides the search using a binary search tree.

15. The search engine as described in claim 14, wherein the priority controller, through utilization of the address cache enables parallel execution of a search operation and an edit operation as performed by the search module and edit module respectively.

16. The search engine as described in claim 14, wherein the search module is communicatively connected to a second search module of a second search engine position at a neighboring level, the second search engine positioned at least one of at a previous or subsequent level to the search module.

17. The search engine as described in claim 14, wherein the edit module has inputs and outputs from a neighboring search engine level to the search engine.

18. The search engine as described in claim 14, wherein the priority controller gives priority to a search operation over an edit operation.

19. The search engine as described in claim 14, wherein the priority controller accesses the address cache to provide parallel access.

20. The search engine as described in claim 19, wherein the priority controller receives a request to read a memory address of the memory, content of the memory address is copied to a first cache address and a second cache address of the address cache.

21. A system suitable for providing a search, comprising:

a central controller suitable for implementing search and edit operations, the central controller suitable from inputting and outputting external communications; and

a plurality of search engines arranged in zero through *k* levels, wherein *k* level search engine of the plurality of search engines is communicatively coupled to the central controller and a zero level search engine of the plurality of search engines

is communicatively coupled to the central controller, wherein the central controller performs parallel execution of a search operation and an edit operation through utilization of a binary search tree and at least one of the plurality of search engines.

22. The system as described in claim 21, wherein the central controller and the plurality of search engines are communicatively coupled via a search connection, an edit connection and a cache connection.

23. The system as described in claim 21, wherein at least one of the search engines include a priority controller, memory, edit module, search module and address cache.

24. The system as described in claim 23, wherein the priority controller manages access to the memory by the edit module, search module and cache module.

25. The system as described in claim 23, wherein the priority controller accesses data utilizing the address cache, the address cached configured to receive data from the memory.

26. The system as described in claim 23, wherein the edit module connects with the memory through the priority controller, the edit module configured to perform calculations for editing operations and wherein the search module is configured to perform calculation for a search operation.

27. The system as described in claim 26, wherein the search module is communicatively connected to a second search module of a second search engine position at a neighboring level, the second search engine positioned at least one of at a previous or subsequent level to the search module.

28. The system as described in claim 27, wherein the search engine is included in the zero level search engine, output of the search module is provided to the central controller and

wherein the search engine is included in the *k* level search engine, the input of the search module is obtained from the central controller.

29. The system as described in claim 23, wherein the edit module has inputs and outputs from a neighboring search engine level to the search engine.

30. The system as described in claim 23, wherein the priority controller gives priority to a search operation over an edit operation.

31. The system as described in claim 23, wherein the priority controller accesses the address cache to provide parallel access.

32. The system as described in claim 31, wherein the priority controller receives a request to read a memory address of the memory, content of the memory address is copied to a first cache address and a second cache address of the address cache.